

# Automatic Gain Control (AGC)

Usage of the Automatic Gain Control Circuit

TDA520x, TDA521x, TDA522x,  
TDA7200, TDA7210 and TDA7210V

ASK and ASK/FSK Superheterodyne Receivers (SHR) for the sub 1 GHz  
frequency bands

## Application Note

Revision 1.1 , 2010-09-07

**Edition 2010-09-07**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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**Automatic Gain Control (AGC)**

Revision History: 2010-09-07, 1

Previous Revision: V1.0, 2009-09-21

Page	Subjects (major changes since last revision)
	TDA72xxV types added
	More detailed description of the methodes

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Last Trademarks Update 2009-05-27

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## 1 Introduction

The TDA520x, TDA521x, TDA522x, TDA7200, TDA7210 and TDA7210V receivers provide an AGC (Automatic Gain Control) circuit that can be used in the active mode, or in the inactive low gain mode to extend the dynamic range of the receiver. The output stage of the mixer has a fixed bias current of 300  $\mu\text{A}$  that is required to drive a CER filter load of 330  $\Omega$ . The internal 300  $\mu\text{A}$  constant current source means that signal from the IF output, that has a peak voltage of 100 mVp (70 mVrms), driving a load of 330  $\Omega$  is already starting to become non-linear. Assuming a voltage gain of 40 to 50 dB from the antenna to the IF output, a good starting point for to enable the AGC circuit is -70...-60 dBm. The action of asserting the LNA in the low gain mode will reduce the subharmonic interferers of 10.7 MHz IF. Without the AGC circuit the current through the output of the mixer stage is starved for strong signal conditions, thus harmonics the 10.7 MHz IF can be created at the IF output.

Another method to reduce the subharmonic interferer is to increase the bias current in the mixer output stage (IFO at pin-12). Increasing the bias current can be accomplished by placing a resistor from the IFO to ground. By adding a shunt resistor of 1.2 k $\Omega$  the IIP3 of the LNA and Mixer stages is increased by ~9 dB at 434 MHz for instance.

Note: The pin numbers indicated in this document are valid for all types except the TDA7210V.

At the TDA7210V pin "TAGC" is pin 2 (pin 4 at all other types) and pin "IFO" is pin 10 (pin 12 at all other types).

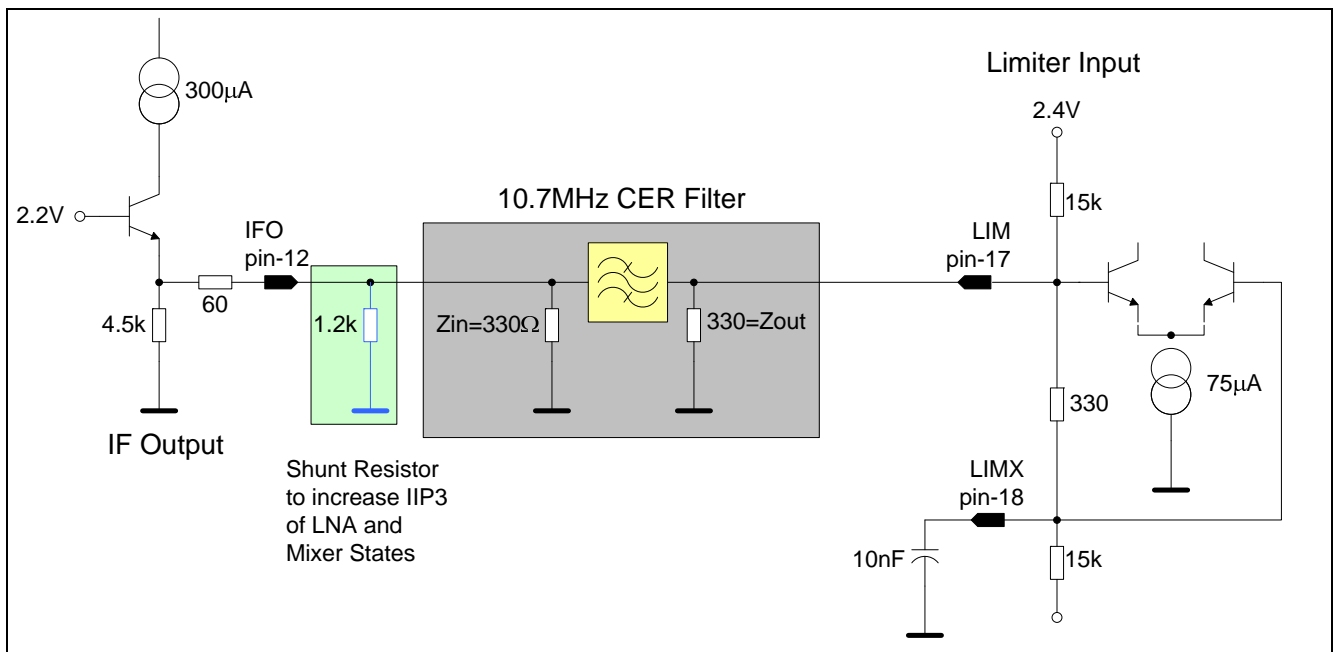


Figure 1 IF Output stage driving the 330  $\Omega$  impedance of the 10.7 MHz CER Filter

## 2 AGC Active Mode

In the active mode the Receiver Signal Strength Indicator (RSSI) voltage is compared with a reference voltage applied on pin 23 of the receiver ( $V_{THRES}$ ). The RSSI voltage is generated by summing current from the logarithmic Limiter Amplifier. The resulting RSSI voltage is then proportional to the power applied at the Low Noise Amplifier input (LNI). The voltage for  $V_{THRES}$  can be derived from a resistor divider that uses the precision +3 V output from pin 24 of the receiver. When the RSSI signal is higher than  $V_{THRES}$  the Operational Transconductance Amplifier (OTA) will source a current of 4.2  $\mu\text{A}$  into an external capacitor at pin 4 of the receiver (TAGC), which causes a reduction of gain. Whereas a RSSI signal voltage below  $V_{THRES}$  will cause the OTA to sink current of 1.5  $\mu\text{A}$  from the capacitor on TAGC. The relative large charge current (RSSI >  $V_{THRES}$ ) means a fast reduction of the LNA gain, known as fast attack. The LNA gain can be reduced by maximum ~20 dB. The much smaller discharge current of only 1.5  $\mu\text{A}$  (RSSI <  $V_{THRES}$ ) means a slow release (slow decay) and bridges logic zeros of an OOK (ASK) signal, where no RF-power is received. The value of the capacitor connected to pin 4 determines the attack and decay time of the AGC and has to be adjusted according to the data rate of the received signal.

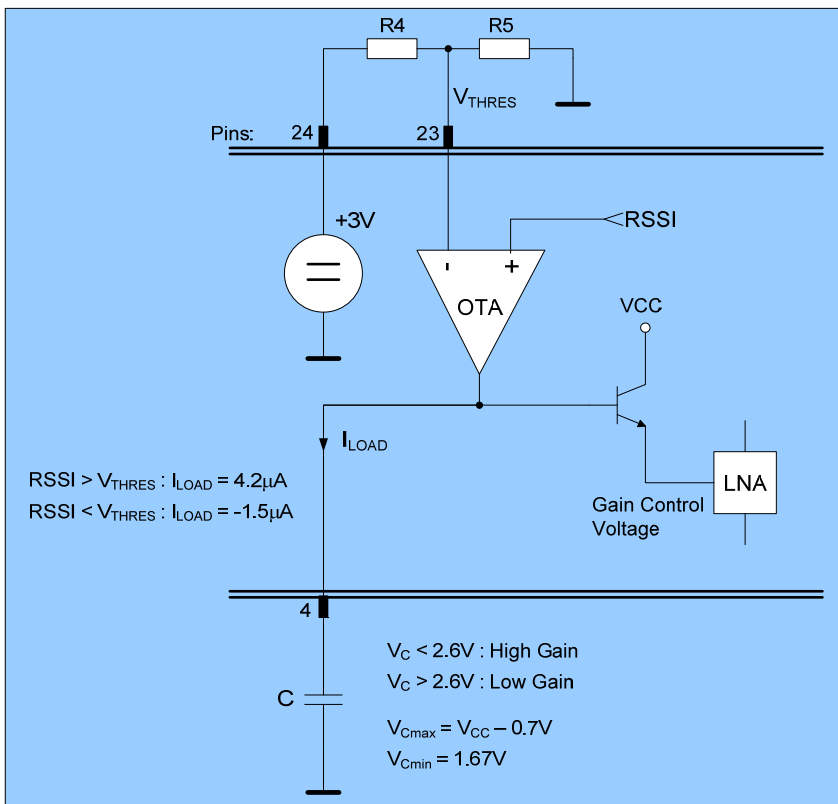


Figure 2 AGC Control Loop Block Diagram

The action of sourcing or sinking current from the OTA generates a DC voltage on the capacitor connected to pin 4 correlating to the RF input power. A voltage across the capacitor ( $V_{TAGC}$ ) of less than 2.6 V forces the LNA into the high gain mode, whereas a voltage higher than 2.6 V forces the LNA into low gain mode. This is shown in Figure 3 where  $V_{THRES} = 1.85\text{V}$ . When the RSSI reaches  $V_{THRES}$  (~ -83 dBm) the voltage at pin 4 ( $V_{TAGC}$ ) rises to 2.6 V, which means that the AGC starts to reduce the gain of the LNA. That's why a further increase of the input level up to ~ -63 dBm does not cause a further increase of the RSSI-signal. So the AGC keeps the RSSI-signal almost constant over an RF-input level range of ~20 dB by reducing the gain of the LNA up to 20 dB. Above a RF-input level of -63 dBm the RSSI-signal increases with the same steepness as below the threshold (in high gain mode), whereas the voltage  $V_{TAGC}$  increase to 4.4 V where it is then internally clamped. At the end of the dynamic range of the Limiter Amplifier become saturated and the RSSI voltage stays almost constant.

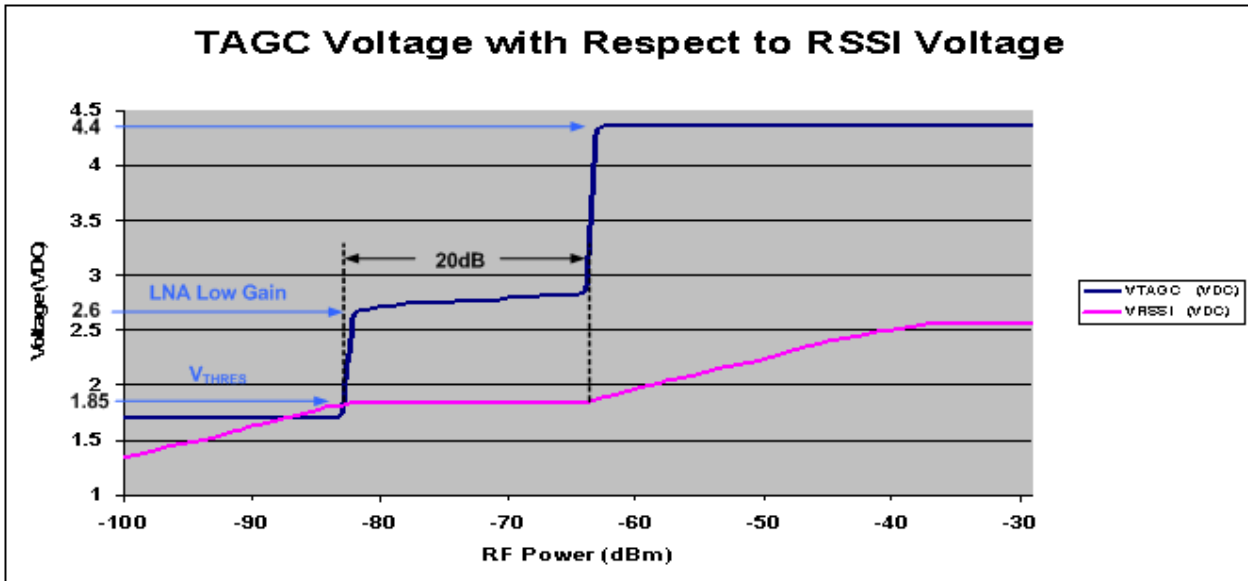


Figure 3 TAGC voltage with respect to the RSSI voltage



### 3 Setting the RSSI Threshold

The SNR of a received signal on the demodulator input is higher the higher the RF-level of the received signal and the lower the system noise figure of the receiver. As the system noise figure (NF) increases and consequently the SNR decreases with decreasing gain of the LNA, the gain of the LNA should be as high as possible for RF-signals showing a very small level, to reach the maximum sensitivity.

Consequently the threshold of the AGC (RF-level where the AGC starts to reduce the gain of the LNA) should be sufficiently high to reach a reasonable SNR above the threshold level. On the other hand the threshold level should be low enough to reduce the gain before the signal distortion exceeds a certain level.

Assuming a sensitivity of -110 dBm for instance, a threshold in the RF-range between -60 dBm and -70 dBm yield a sufficient high SNR when the AGC reduces the gain, as the AGC starts to reduce the gain not before the RF-input level is 40 to 50 dB or more above the sensitivity level. In addition the distortion of the signal at -70 dBm to -60 dBm is rather small, so the AGC will keep the distortion small over a certain range above the threshold level.

To set the threshold voltage to a value corresponding to a RF-input level 40 dB to 50 dB above the sensitivity limit, an RF-input signal has to be applied on the RF-input (antenna) which is 40 dB to 50 dB higher than the sensitivity limit. The voltage which can be measured now on the Peak Detector output (PDO) is equal to the RSSI voltage applied on the non-inverting input of the OTA of the AGC. That's why this voltage should be applied on pin 23 (THRES) to get a threshold voltage corresponding to a RF-level 40 dB to 50 dB above the sensitivity limit. A voltage divider connected to the 3 V reference output at pin 24 can be calculated to provide the desired threshold voltage ( $V_{\text{THRES}}$ ) at pin 23. The net sum of the resistor divider is recommended to be 600 k $\Omega$ .

## 4 AGC Inactive Mode

The inactive mode means that the LNA is forced either to high gain mode or to low gain mode independent of the RF-signal level.

### 4.1 Low Gain Mode

The low gain mode is achieved by asserting a voltage to pin 23 such that  $V_{THRES}$  is 0 to 0.7 V. This can easily be achieved by simply connection pin 23 to ground. This could be actively controlled as well by setting the port of a microcontroller low. In the low gain mode the dynamic range of the receiver can be extended and the risk of distortion due to an interferer could be reduced. This mode may be desired if an external LNA with a low Noise Figure (NF) is used on the front-end of the receiver to improve the sensitivity. Setting the LNA in the low gain mode should be considered if the gain of the external LNA is more than 12 dB, because the overall CP1dB through the receiver frontend is decreased by the additional gain. Additionally the high over all gain and poor PCB layout could comply with the condition for oscillation due to cross coupling between the output of the LNA (LNO) and the input of the external LNA. Consequently the LNA input of a possibly used external LNA should not be placed close to the output of the internal LNA. So these circuits should be arranged more in a row than in a circle. The capacitor at pin 4 is required also in case of forcing the LNA to low gain mode, of course!

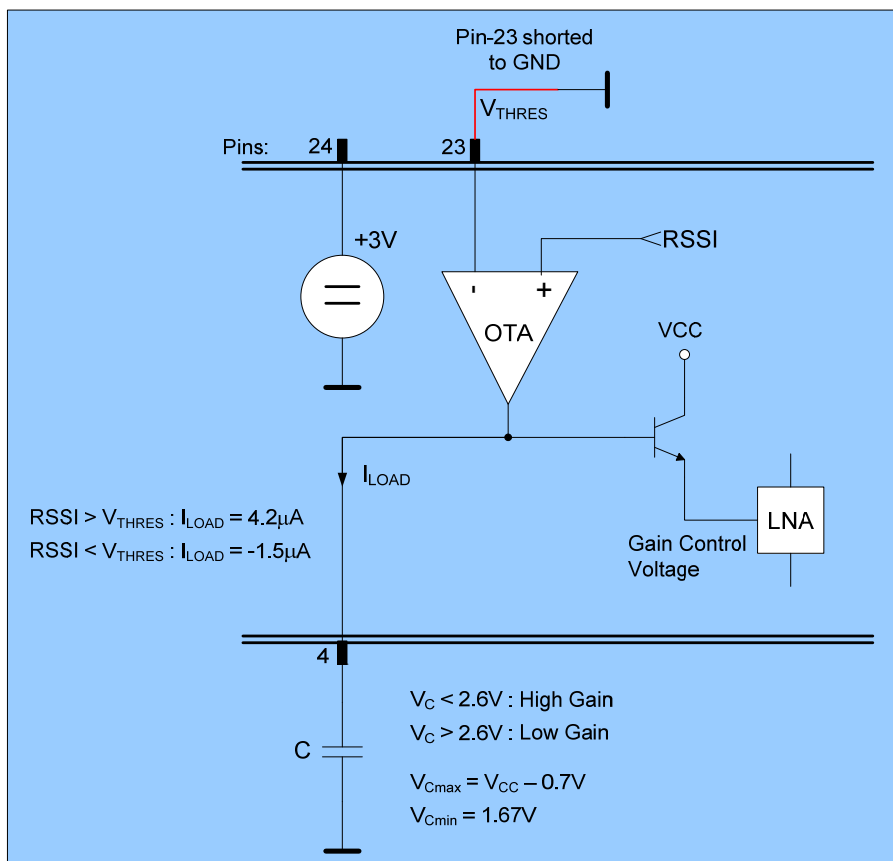


Figure 4 Forcing the LNA in the low gain mode

## 4.2 High Gain Mode

### 4.2.1 Forcing the TDA521x, TDA522x, TDA7200, TDA7210 or TDA7210V in high gain mode

The LNA can be forced in high gain mode by applying a voltage on pin 23 (THRES), the inverting input of the comparator (OTA), higher than the RSSI voltage. The LNA can be forced reliable and independent of the RF-input level in the high gain mode by setting the condition  $V_{THRES} > 2.8\text{ V}$  to  $V_{CC} - 1\text{ V}$  in case of TDA521x, TDA522x, TDA7200, TDA7210 and TDA7210V. So the LNA can be forced in the high gain mode by connecting pin 23 (THRES) directly to pin 24 (3VOUT), the precision 3 V output (see Figure 5). Of course a capacitor is required at pin 4 also when forcing the LNA in the high gain mode to prevent toggling between high gain mode and low gain mode.

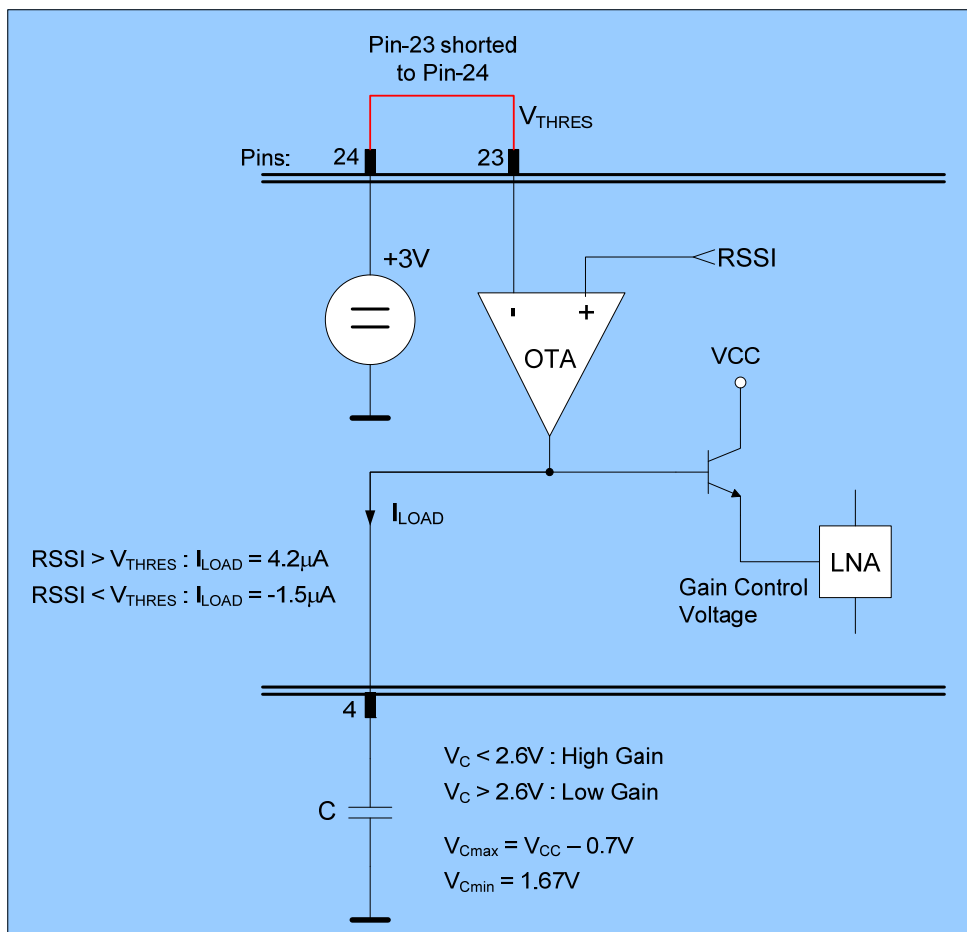


Figure 5 Forcing the LNA of TDA521x, TDA522x, TDA7200, TDA7210 or TDA7210V in the high gain mode

#### 4.2.2 Forcing the TDA5200 or TDA5201 in High Gain Mode

The LNA of the TDA5200 and TDA5201 could be forced in high gain mode by applying a voltage of 3.3 V or higher on pin 23 (THRES). On the other hand the voltage must not be higher than  $V_{CC} - 1$  V, so a DC-voltage between 3.3 V and  $V_{CC} - 1$  V would be required. Fortunately there is also another possibility, getting by with the 3 V from pin 24, to force the LNA in high gain mode also for the TDA5200 and TDA5201. The LNA of all types described here can also be forced into the high gain mode by connecting pin 23 to pin 24 as shown in Figure 5, but connecting pin 4 directly to ground in addition instead of connecting a capacitor on pin 4. In addition this can be a cost savings to the receiver design and can also increase the ESD robustness at pin 4. Connecting pin 4 to ground will assure that the LNA will be in the high gain mode regardless of the amplitude of the RSSI voltage and consequently regardless of the RF-input signal level for all types of receivers described in this Application-Note.

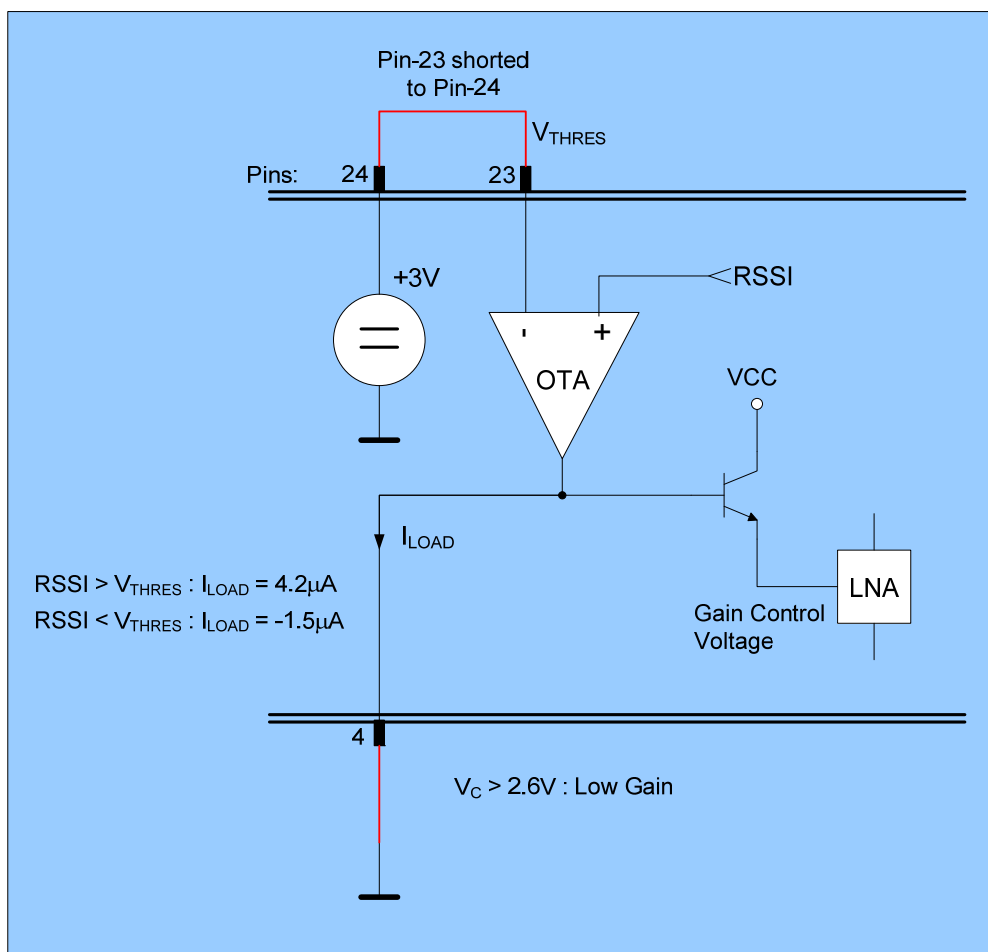


Figure 6 Forcing the LNA in the high gain mode with pin 4 grounded

## 5 RSSI Curves for Active and Inactive Modes

As already explained in chapter 3, the inactive mode means that the LNA is either forced to high gain mode or to low gain mode regardless of the RF-input level. In active mode the threshold of the AGC is set to a voltage which is anywhere in-between the RSSI voltage range. The range where the AGC is active means the RF-input level range within the AGC is able to reduce the gain further with increasing RF-input level, so the range within the AGC keeps the RSSI voltage almost constant. The RSSI curves in Figure 7 show the RSSI-voltage over the RF-input level and how the dynamic range of the receiver can be increased by using the AGC circuit in the active mode. When the LNA is forced to high gain mode, the AGC circuit is inactive over the whole RF-input level range and the dynamic range of the receiver is consequently reduced by 20 dB. Incipient from above the noise floor up to saturation the slope of the RSSI voltage is always the same, both in high gain mode and in low gain mode, except the range where the AGC is active.

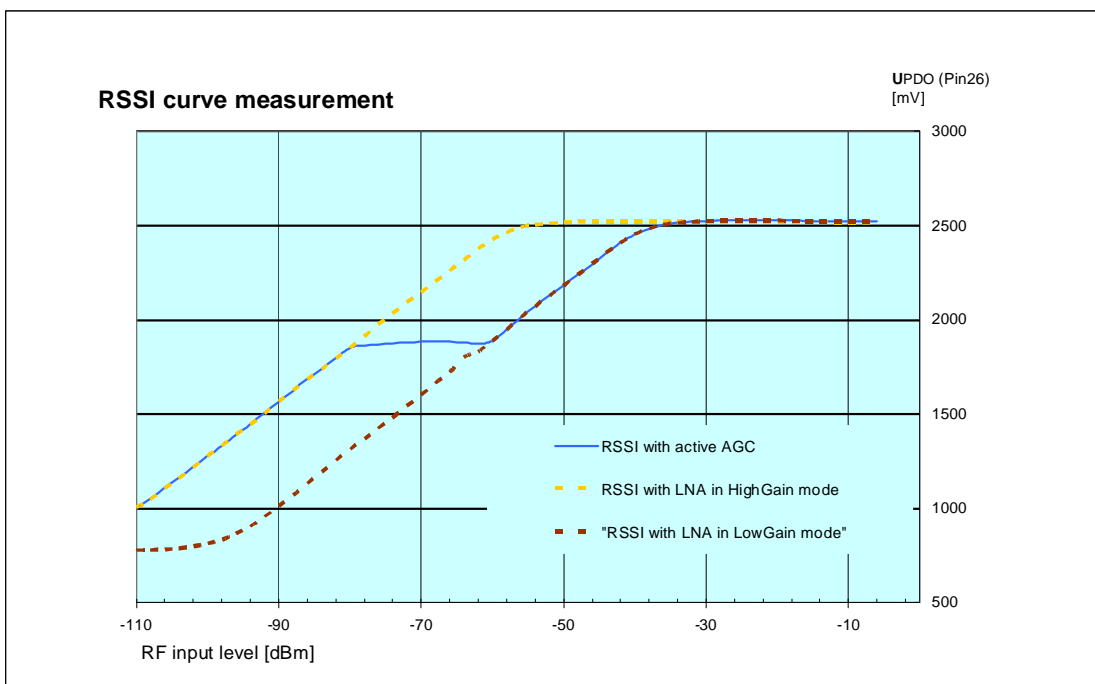


Figure 7 RSSI curves for active and inactive modes

## 6 Conclusion

To use the AGC circuit in the active mode the threshold voltage ( $V_{THES}$ ) at pin 23 needs to be set such that when the AGC starts reducing the gain the SNR is sufficiently large and significantly larger than at the sensitivity limit. Also the capacitor used at pin 4 should be set such that the time constant associated to the fast attack and slow decay is appropriate for the data rate of the receiver in the given application.

In the inactive mode the LNA can be forced into the low gain mode by connecting pin 23 to ground, or asserting a voltage to pin 23 that is at least lower than 0.7 V. The dynamic range of the receiver can be extended by ~20 dB by using the receiver in the active mode. Also by using a shunt resistor from pin 12 (IFO) to ground the IIP3 of the LNA and mixer stages is increased by ~9 dB at 434 MHz for instance.

The LNA can alternatively be forced into the high gain mode by connecting pin 23 directly to pin 24 and pin 4 directly to GND. This would save a capacitor in addition.

**In no case can pin 4 be left open in the active or inactive modes of operation.**

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